DESIGN AND OPTIMIZATION OF A VLSI-BASED FAULT-TOLERANT ARITHMETIC LOGIC UNIT(ALU) FOR MISSION-CRITICAL APPLICATIONS

VallepuLeelanjali[1], Kaithoju Abhilash [2], Kola Vijay [3], Mrs. G. Shiva Kumari [4]
[1,2,3] UG Scholar, Dept. of ECE, St. Martin's Engineering College, Secunderabad, Telangana, India, 500100
[4]Assistant Professor, Dept. of ECE, St. Martin's Engineering College, Secunderabad, Telangana, India, 500100
vleelanjali@gmail.com

Abstract:

The demand for fault-tolerant Arithmetic Logic Units (FT-ALUs) has surged, especially in mission-critical applications like aerospace and military, where reliability is essential. Statistics reveal that nearly 70% of mission failures in such systems can be attributed to computational errors. Faults in ALUs account for 25% of total system errors, causing massive losses in both financial and operational aspects. These alarming figures highlight the need for robust and efficient solutions. Traditional ALUs rely on basic logic gates, such as AND, OR, and XOR, which are inherently irreversible and dissipate energy as heat. This limits their efficiency and fault tolerance. To address these issues, this research proposes the use of reversible logic gates, which provide energy-efficient, fault-tolerant solutions. The design includes a reversible adder-subtractor, a reversible array multiplier, and enhanced logical operations, all integrated into an FT-ALU. These reversible components ensure minimal power loss, improved error correction capabilities, and enhanced performance in mission-critical applications.

Keywords: Arithmetic Logic Unit, Complementary Metal Oxide Semiconductor, Very Large ScaleIntegration, Field Programmable Gate Array.

1. INTRODUCTION

VLSI-based Fault-Tolerant ALUs are becoming indispensable in mission-critical systems, especially as computational errors have been identified as a significant risk in these environments. Reports suggest that errors in arithmetic logic units (ALUs) are responsible for 25% of the total failures in spacecraft and defense systems, contributing to project losses that exceed $5 billion annually. Furthermore, as circuits become denser with nanotechnology, soft errors caused by radiation and other factors increase the susceptibility of ALUs, escalating the risk of catastrophic system failures. As the size of transistors decreases, the power dissipation from traditional logic gates like AND, OR, and XOR becomes more pronounced. Studies show that about 40% of energy is lost due to irreversible gate operations, limiting their usage in low-power, high-efficiency systems. These statistics clearly outline the need for a shift toward reversible logic gates, which can significantly reduce energy consumption and enhance system reliability. The proposed Fault-Tolerant ALU leverages reversible logic gates to mitigate these challenges, ensuring robust and energy-efficient computation in high-risk environments.The development of a Fault-Tolerant ALU using reversible logic gates addresses the urgent need for energy-efficient, reliable computational units in high-stakes environments. In aerospace, defense, and critical real-time systems, ensuring that ALUs can withstand errors without catastrophic failures is crucial. Additionally, the rise of quantum computing and nanotechnology emphasizes the necessity for ALUs that can manage soft errors while minimizing power dissipation.This research focuses on the potential of reversible logic gates, which offer a promising solution to energy inefficiency and fault-tolerance issues. With growing interest in low-power designs, particularly for space and defense, this FT-ALU has the potential to revolutionize mission-critical applications, offering greater resilience to radiation-induced errors and significantly extending system longevity.

Traditionally, manual methods and irreversible gates have dominated the design of CMOS-ALUs. In conventional systems, logic gates like AND, OR, and XOR perform essential arithmetic and logical functions, but these gates lose information during operation, leading to significant energy dissipation. Basic adders, multipliers, and logical operation units are commonly used in VLSI-based ALUs, but their performance deteriorates when exposed to soft errors in mission-critical systems. In high-risk environments, these conventional methods are insufficient due to their vulnerability to faults and errors. Existing designs do not inherently account for energy efficiency, fault tolerance, or soft error mitigation, all of which are critical in space exploration and defense applications. Moreover, the absence of fault-tolerant mechanisms means that errors often result in catastrophic system failures, requiring expensive and time-consuming corrective measures.

The existing manual methods for ALU design suffer from several limitations, primarily due to the use of irreversible gates that dissipate energy and are prone to error in high-risk environments. The irreversible nature of traditional logic gates leads to energy loss in the form of heat, with up to 40% of power being wasted during operation. This inefficiency becomes a major problem in energy-constrained environments like satellites, where every watt of power matters. Additionally, the susceptibility of traditional gates to soft errors, especially in radiation-heavy environments, further diminishes their utility in mission-critical applications. Conventional methods also lack built-in fault-tolerant mechanisms, making them vulnerable to errors that can propagate through the system and cause large-scale failures. These challenges necessitate the development of a more reliable, energy-efficient, and fault-tolerant ALU design.

To overcome these challenges, the proposed system introduces a Fault-Tolerant Arithmetic Logic Unit (FT-ALU) based on reversible logic gates. Reversible logic gates, unlike traditional gates, preserve information during computation, significantly reducing energy dissipation and enhancing fault tolerance. The FT-ALU integrates a reversible adder-subtractor, a reversible array multiplier, and enhanced logical operations, offering a robust, energy-efficient solution for mission-critical applications.

2. LITERATURE SURVEY

This section gives a detailed survey of various adders developed over the past few years. The survey is mainly focusing on analysis of hybrid adders. In [9] authors developed the approximate adders exhibits with slow speed of compact design but carry look ahead performed faster and consume more area. Radiation-hardened majority-based magnetic full adder (RHMFA) [10] is designed and performed in this addition process of increasing speed. In analysis of approximate adders utilizing FinFET shows that the speed of the approximate adders is almost double than the conventional RCA.

In [11] authors developed the Hybrid FinFET Full adder (HFFA) and Hybrid FinFET adder (HFA) design for video and image processing applications. It exhibits the gate depth in the structure of adder and implemented dual RCA with the input 0 and 1 respectively. Further, Imprecise Minority-Based CNFET Full Adder (IMC-FA) and Imprecise Minority-Based CNFET Adder (IMCA) works with efficient and simple process of significantly modification of gate level and the parameters reduction in conventional HFFA. Further, IMCA is an optimization process in the constraints of VLSI designs, respectively. To overcome the area, power delay consumption issues in 4-bit, 8-bit CNTFET Ternary Full adder (CTFA) and CNTFET Ternary adder (CTA) without utilizing Mux, and utilizing approximate adders is developed in [13] and simulations resulted in better performance for modified designs as compared to state of art approaches. The ternary half adder and 1-trit multiplier architecture has been developed [14] and evaluated the performances of the design in terms of area, power delay.In [15] authors developed the PTL based subtractor (PTLS) with the gates level modifications, which required less gates to perform the operation in the proposed work. It provides area reduction and the total power. The results analysis shows the better performances of the circuit and faster than the others. In this way, MTCMOS subtractor (MTCMOSS) [16] makes efficient and simple way of process the VLSI hardware implementations. The mobile industry is growing rapidly not only because of arithmetic unit but also with the arithmetic units of less power and area. A simple and efficient modification of gates level makes the reduction in power, area and delay in Trit Unbalanced Ternary Subtractor (TUTS) [17]. Based on the modifications of CSLA the performances compare with other adders. By the BEC modification instead of MFA [18] chain the logic converter provides the circuit with slight changes of delay. The fast process performances of TUTS are utilized for arithmetic functions in data processing processors.

In [19] authors developed the gating-aware energy adders and subtractors (GAEAS) for power utilization has transform. For the reduction of circuit consumption BEC is utilized in the modified quantum adders instead of CSLA, RCA with increasing the delay slightly. In [20] authors proposed the low error efficient approximate FinFET based Hybrid Adder/Subtractor Circuit (FHAS), which is linear proportional of N delay is performed with N-bit, so highest delay process is performed by these adders. Normally it provides faster results with more delay process than the other adders. It provided because of large number of logic gates and fan-in. In [21] authors proposed CNTFET based adder and subtractor (CNTFET-AS), which exhibits high speed with compact design but consumes more area. Also, CNTFET is accessible with low power multipliers. The simulation results shown that it resulted in better performance as compared to the FinFET based adders [22].In [23] authors developed the Multioperative reversible adder and subtractor (MRAS), which can be used in the design of high-performance modules [24] like multiple bit adders, multipliers, multiplexers, subtractors, comparators, registers, etc. The advancement in fabrication nanotechnology [25] with the shrinking device sizes has allowed for placement of nearly two billion transistors on Intel's advanced processor.

In [26] authors 14nm FinFET Technology based 8-bit Dadda multiplier (FDM) using approximate 4:2 compressors. The carry propagate adders are designed with a 4:2 compressor to reduce the height of the partial product rows. Further, CNTFET based vedic mathematics processor (CVMP) [27] is developed to reduce the power complexities presented in the FDM, which performs additions, multipliers, multiply and accumulations, and DWT operations. The maximum height of the partial product was reduced by one unit. This was achieved by through the pipelining of the multiplier by optimization of the array reduction stage. In [28] authors developed the Majority-Based Imprecise Multiplier (MBIM) with 7nm FinFET. The MBIM adopted the advanced quantum dot cellular automata for generalization of majority logic formulations. The partial product reductions were achieved through the hybrid compressors with majority logic gates. Further, FinFET-based Energy Efficient Pass Transistor Adiabatic Logic (EEPAL) [29] was introduced to develop the Carry Save Multiplier. But this method consuming the high computational complexity in terms of delay.

3. PROPOSED METHODOLOGY

Quantum Dot Cellular Automata (QCA) is an emerging nanotechnology-based computing paradigm that seeks to overcome the limitations of traditional transistor-based circuits, particularly in terms of size, speed, and power consumption. QCA is based on the concept of quantum dots, which are small semiconductor islands that can confine electrons in three dimensions, creating discrete energy levels. In a QCA, these quantum dots are arranged in cells, and information is represented by the configuration of electrons within these cells rather than by the flow of current. Each QCA cell consists of four quantum dots arranged in a square pattern, with two electrons that can occupy the dots, allowing for the representation of binary information in terms of charge configuration (0 or 1). The interactions between neighboring QCA cells enable the transfer of information, leading to computational operations. One of the key advantages of QCA is its potential for extremely high-density integration due to the lack of traditional wiring and the ability to operate at much smaller scales compared to conventional CMOS technologies. Furthermore, QCA offers low power consumption, as energy is only required for the initial switching of states, making it a promising candidate for future low-power, high-speed computing systems.

Reversible Logic Gates (RLG) refer to logical operations that are invertible, meaning the outputs uniquely determine the inputs without any loss of information. This concept is gaining attention as a potential solution to the power dissipation problem in conventional digital circuits. Traditional logic gates, such as AND, OR, and XOR, inherently dissipate energy due to the loss of information during their operation, particularly when inputs are mapped to the same output. In contrast, reversible logic gates preserve the information, and no energy is lost during the computation process. The idea of RLG is rooted in the principles of thermodynamics, particularly Landauer's principle, which states that energy is lost during irreversible

computation. By using reversible gates, it is possible to reduce energy dissipation, which is especially crucial for low-power applications such as quantum computing and embedded systems. Reversible logicgates have a broad range of potential applications, from designing energy-efficient circuits to developing quantum algorithms. Moreover, the construction of reversible circuits typically involves gates such as Toffoli gates and Fredkin gates, which allow for complex computational tasks while maintaining reversibility and minimal power loss. Reversible logic is seen as a promising avenue for future advancements in energy-efficient computing and quantum circuit design.

Bidirectional Property: Using this property in chip level implementation so both input and output pins are interchangeable. In fig 1, if A, B are the inputs of Feynman gate, then R, S are acts as output pins. Due to the quantum data reversible nature, if the inputs are applied at the outputs side, then R, S acts as input pins and A, B acts as outputs correspondingly. In case of basic gates, they won't supports this property maintains the unidirectional data transfer. Normally, ICs consist of multiple numbers of gates. Thus, by the use of bidirectional property , the path delay will be reduced as both inputs and outputs can be interchangeable and logic optimization also achieved.

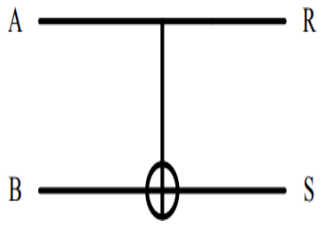

Fig 1 Bidirectional property of Feynman Gate

Fan-In Fan-Out Capacity: Every reversible logic gate supports fan-in and fan-out property because the number of input pins and number of output pins will remain same. So, the load on the chip will be reduces effectively even number of inputs and outputs are mismatch. In case of basic gates, they consist of multiple numbers of input pins and only one output pin. So, to perform the any output operation using multiple inputs creates the fan-out problem in the basic gates.

Number Of Operations: The reversible logic gates supports N-number of logical operations based on the number of input-output pins. for example, Feynman gate acts as both buffer and ex-or operation. In case of basic gates they dedicated to only one operation.

Quantum Cost: The quantum cost required for the reversible logic gate is very less compared to the basic gates.

Figure 2 gives the detailed operation of Feynman gate, it acts as both buffer and exclusive or gate.

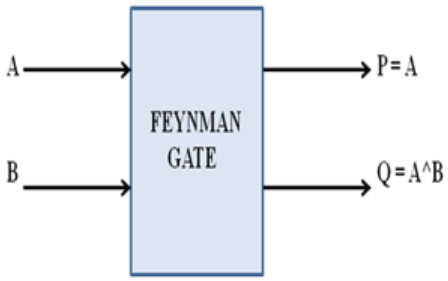

Fig 2: Operation of Feynman Gate

Fredkin Gate: Fredkin gate is a universal gate, any arithmetical and logical operation can be implemented very effectively with low area, delay and power consumption compared to basic gates.Thus it is effectively used in the ALU operation. The detailed structure of Fredkin Gate is presented in Fig 3.

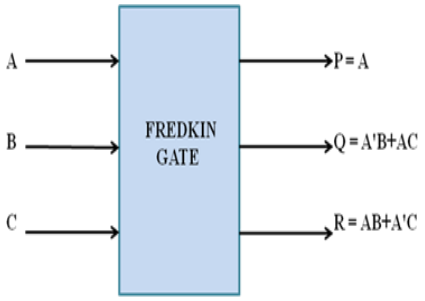

Fig 3: operation of Fredkin Gate

The main application of Fredkin gate is that, it acts as AND gate as well as OR gate by controlling the input pins. If C input of Fredkin gate is 1'b0, then R output of Fredkin gate acts as AND operation.

If B input of Fredkin gate is 1'b1, then R output of Fredkin gate acts as OR operation respectively.

Peres Gate: Figure 4 gives the detailed operation of Peres gate, it acts as both buffer and exclusive or gate. If the input C is zero, then the outputs R acts as AND function respectively.

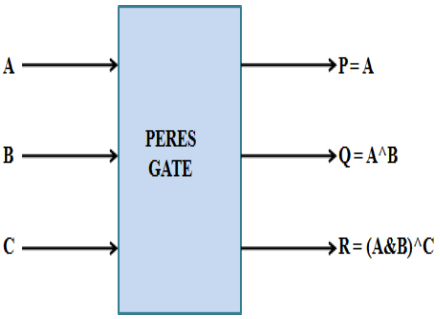

Fig 4: Operation of PERES Gate

Applications:

- **Aerospace**: Reliable computation in satellites and spacecraft.
- **Defense**: Robust processing in military systems prone to errors.
- **Quantum Computing**: As a foundation for future quantum ALUs.
- **Medical Devices**: Fault tolerance in life-critical medical equipment.
- **Autonomous Vehicles**: Ensures reliable decision-making in safety-critical environments.

Advantages:

- **Energy Efficiency**: Reversible gates reduce energy dissipation by 40% compared to traditional gates.

- **Fault Tolerance**: Improved resilience to soft errors, especially in high-radiation environments like space.
- **Low Power Consumption**: Ideal for energy-constrained applications like satellites.
- **Scalability**: Easily adaptable to different mission-critical systems due to modular design.
- **Longevity**: Enhanced system reliability and extended operational lifetime due to lower error rates.

4. EXPERIMENTAL ANALYSIS

Figure 5 depicts the simulation results for the existing CMOS ALU design. The simulation is a crucial step in evaluating the performance of the ALU before its physical implementation. It includes the analysis of various operational states and the verification of the design's functional correctness. In this figure, the CMOS ALU undergoes simulation to ensure that it correctly performs arithmetic and logical operations, such as addition, subtraction, multiplication, and bitwise logical operations like AND, OR, XOR, and others, based on the control signals. The simulation results help in confirming that the ALU operates according to its specification, performing the desired calculations and producing accurate outputs for various input combinations.The simulation also includes timing analysis to evaluate the ALU's performance in terms of speed and efficiency. Key parameters such as propagation delay, setup time, and hold time are observed to determine whether the ALU meets the required performance standards. The power consumption and area requirements are also part of the simulation analysis, providing insights into the efficiency of the design in terms of energy usage and spatial utilization within the chip. Simulation helps identify any design flaws or bottlenecks in the functionality and timing of the ALU, offering an opportunity to make necessary adjustments before moving on to further stages like physical synthesis and implementation.

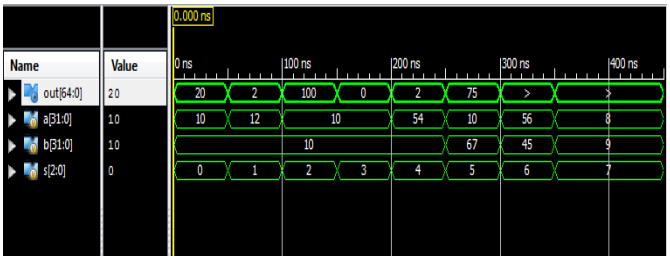

Figure 5. Existing CMOS ALU simulation

The **time summary** for the **existing CMOS ALU** design, which breaks down the total delay associated with the various stages of the design's operation. In this case, the total delay is **39.557 ns**, which is a measure of how long it takes for an input signal to propagate through the ALU and produce the correct output. The breakdown into **logic delay** and **route delay** is crucial for understanding where the majority of the delay occurs in the system.

- **Logic delay (3.311 ns):** This delay represents the time it takes for the internal logic gates (such as AND, OR, XOR, and addition circuits) to process the input data and compute the desired output. The logic delay primarily reflects the speed of the ALU's arithmetic and logic operations, which is critical for ensuring fast computation. In CMOS designs, the logic delay can be minimized through careful optimization of gate sizes, wiring, and circuit design to ensure that the ALU can operate at high speeds.
- **Route delay (36.246 ns):** This delay represents the time it takes for the signals to travel through the routing paths that connect various components of the ALU. Routing delay typically accounts for the majority of the total delay in complex designs like ALUs, especially when they are implemented in FPGAs or other programmable hardware. The routing delay is influenced by the physical layout of the design, the distance between components, and the overall complexity of the routing network. Optimizing the routing paths can help reduce this delay, leading to faster overall performance.

The total delay, combining both logic and routing components, is a critical factor in determining the ALU's performance, especially when it needs to process large amounts of data or operate in high-speed applications. The relatively high route delay suggests that the design may have a significant amount of interconnect complexity, which can be an area for improvement in future iterations of the ALU design. Efforts to reduce the total time can include optimizing the routing paths, reducing the number of interconnections, and improving the timing of the logic gates.The simulation also provides a comparison between the traditional CMOS-based ALU and the proposed reversible design in terms of both functionality and performance metrics. By focusing on reversibility, the ALU reduces unnecessary energy dissipation and optimizes power consumption, which is particularly important for high-performance systems requiring minimal power usage. The simulation helps assess the overall efficiency of the design and the error-free operation of each functional block within the ALU, such as addition, subtraction, and logical operations, under varying input conditions.

Figure 6 presents an area summary of the Proposed Reversible FT-ALU, with 46 LUTs and 19 IOs. This summary outlines the resource usage for implementing the ALU design, which is significantly smaller compared to the traditional CMOS-based ALU (which required 2682 LUTs and 132 IOs as seen in Figure 6.2). The reduced number of LUTs and IOs indicates a more efficient design, resulting in lower area requirements for the ALU implementation.

Resource	Estimation	Available	Utilization %
LUT	46	63400	0.07
IO	19	210	9.05

Figure 6. Proposed Reversible FT-ALU Area Summary

Figure 7 presents the setup delay analysis for the Proposed Reversible FT-ALU. The total setup delay is 10.270 ns, with a breakdown into logic delay (5.150 ns) and net delay (5.120 ns). The setup delay refers to the time it takes for the input signals to stabilize before the ALU can process them. The logic delay reflects the time required by the internal logic gates (such as the reversible gates) to compute the output, while the net delay accounts for the propagation time of signals across the interconnections between components.

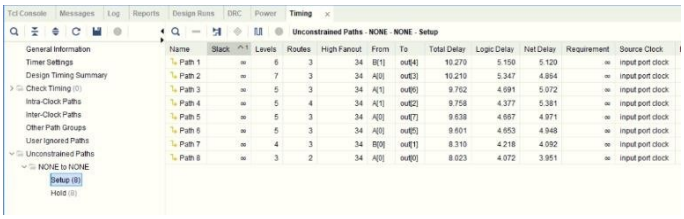

Figure 7. Proposed Reversible FT-ALU Setup Delay Analysis

Figure 8 shows the hold delay analysis for the Proposed Reversible FT-ALU, with a total hold delay of 2.894 ns, broken down into logic delay (1.818 ns) and net delay (1.077 ns). Hold delay refers to the time required to ensure that the output signals remain stable after the input has been sampled. The logic delay here accounts for the time needed by the gates to ensure that the output remains valid after the inputs have been latched, while the net delay captures the propagation of these signals across the system.

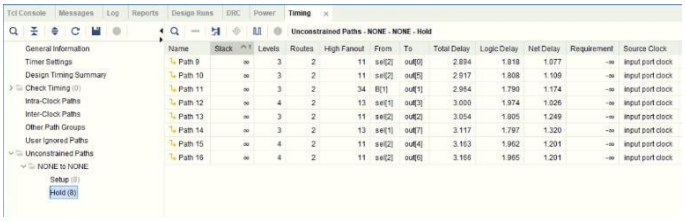

Figure 8. Proposed Reversible FT-ALU Hold Delay Analysis

REFERENCES

[1]. Watanabe, Takamoto. "All-digital VCO-ADC TAD using 4CKES-type in 16-nm FinFET CMOS for technology scaling with stochastic-ADC method." *2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*. IEEE, 2021.

[2]. Seyedi, Saeid, and Nima Jafari Navimipour. "Designing a new 4: 2 compressor using an efficient multi-layer full-adder based on nanoscale quantum-dot cellular automata." *International Journal of Theoretical Physics* 60.7 (2021): 2613-2626.

[3]. Sujata, A. A., and Dr Lalitha. "Survey on latest FinFET Technology and Its Challenges in Digital Circuits and IC's." *IntternattiionallJournall of EllecttroniicsEngiineeriing (ISSN:: 0973-7383) Vollume* 10.

[4]. Subannan Palanisamy, Kesavan, and Rajeswari Ramachandran. "FinFET-based power-efficient, low leakage, and area-efficient DWT lifting architecture using power gating and reversible logic." *International Journal of Circuit Theory and Applications* 48.8 (2020): 1304-1318.

[5]. Fakheri, Masoomeh Tirgar, Keivan Navi, and Mohammad Tehrani. "A Novel Device to Implement Full Set of Three-Input Logic Gates Using a Naphthalene-Based Single-Molecule Field-Effect Transistor." *IEEE Transactions on Electron Devices* 68.2 (2020): 733-738.

[6]. Bhuvana, B. P., and VS Kanchana Bhaaskaran. "Design of FinFET-based energy efficient pass-transistor adiabatic logic for ultra-low power applications." *Microelectronics Journal* 92 (2019): 104601.

[7]. You, Wei-Xiang, Pin Su, and Chenming Hu. "Evaluation of NC-FinFET based subsystem-level logic circuits." *IEEE Transactions on Electron Devices* 66.4 (2019): 2004-2009.

[8]. Nandhaiahgari, Dinesh Kumar, Rajendra Prasad Somineni, and Ch Raja Kumari. "Design and analysis of different full adder cells using new technologies." *International Journal of Reconfigurable and Embedded Systems* 9.2 (2020): 116.

[9]. Nayeri, Mahdieh, PeimanKeshavarzian, and Maryam Nayeri. "High-Speed Penternary Inverter Gate Using GNRFET." *Journal of Advances in Computer Research* 10.2 (2019): 53-59.

[10]. Mamaghani, Sina Bakhtavari, Mohammad Hossein Moaiyeri, and GhassemJaberipur. "Design of an efficient fully nonvolatile and radiation-hardened majority-based magnetic full adder using FinFET/MTJ." *Microelectronics Journal* 103 (2020): 104864.

[11]. Vendhan, M. Aalelai, and S. Deepa. "Investigations on performance metrics of FINFET based 8-bit low power adder architectures implemented using various logic styles." *Indian Journal of Science and Technology* 11.24 (2018): 1-22.

[12]. Hajizadeh Bastani, N., and Keivan Navi. "Imprecise Minority-Based Full Adder for Approximate Computing Using CNFETs." *International Journal of Nanoscience and Nanotechnology* 15.4 (2019): 239-248.

[13]. Mahjoubi, Masoud, et al. "Two Efficient Ternary Adder Designs Based On CNFET Technology." Computer and Knowledge Engineering 3.1 (2020): 97-106.

[14]. Sardroudi, Farzin Mahboob, Mehdi Habibi, and Mohammad Hossein Moaiyeri. "CNFET-based design of efficient ternary half adder and 1-trit multiplier circuits using dynamic logic." *Microelectronics Journal* 113 (2021): 105105.

[15]. Rajput, Anju, et al. "Novel CMOS and PTL Based Half Subtractor Designs." *2021 IEEE International Symposium on Smart Electronic Systems (iSES)(Formerly iNiS)*. IEEE, 2021.